REMARKS/ARGUMENTS

These remarks are in response to the Office Action dated April 25, 2005. Claims 1-18 are pending in the present application. Claims 19, 20 and 21 are new. Accordingly, claims 1-21 are currently pending.

Allowable Subject Matter and New Claims

The Examiner indicates that claims 3-5, 8-12 and 14-18 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, claim 19 incorporates the limitations of claims 1-3, claim 20 incorporates the limitations of claim 6-8 and claim 21 incorporates the limitations of claims 13 and 14. Applicants respectfully submit that claims 19, 20 and 21 are allowable.

Claim Rejections

In the Office Action, the Examiner rejected claims 1, 2, 6, 7 and 13 under 35 U.S.C. §102(b) as being unpatentable over Doblar et al. (U.S. Patent No. 6,338,144). In so doing, the Examiner stated:

> In claim 6, Doblar et al. teaches all claimed features in Fig. 1, a circuit comprising: a clock signal source (12) providing a differential clock signal (Ck, /Ck); and a configurable buffer circuit (16) for receiving the differential clock signal and providing a clock signal output for a plurality of load circuits (20a-20c), wherein the configurable buffer circuit achieves a constant bandwidth (col. 4, line 28; uniform propagation delay result in constant bandwidth) and voltage level for the clock signal output while adjusting to alterations (selected electrical impedances; col. 4 line 28) in the number of load circuits coupled to the configurable buffer circuit, wherein noise immunity is increased (noise immunity is greatly improved; col. 6, line 27).
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> In claim 7, Doblar et al. further teaches the circuit fo claim 6 wherein the configurable buffer circuit (16) further comprises a differential amplifier circuit (26) including a programmable ouput impediance circuit (28) and programmable current source circuit (1).

Applicants respectfully disagree.

The present invention is directed to increasing noise immunity for clocking signals in high speed digital systems. Referring to Figure 2 of the present invention, clock buffering in accordance with the present invention utilizes a single clock source 20, and *a single buffer circuit* 22, where the single buffer circuit 22 is configurable and controlled via an impedance/current control circuit 24 for N number of load circuits 26a, 26b, ... 26n. According to the present invention, the single buffer circuit 22 includes a differential amplifier that has a programmable output impedance and a programmable current source controlled by control signals of the impedance/current control circuit (see FIG. 3). By adjusting the programmable current source and output impedance together, a constant output voltage from the differential amplifier circuit can be achieved regardless of the number of load circuits. Because the present invention does not utilize multiple stages of serial buffering, the number of load circuits receiving the clock signal can be increased as desired without increasing the noise.

While Doblar is also directed to increasing noise immunity, Doblar does so in a completely different manner. In Doblar, *a plurality of buffer circuits 26a-26d* are used to pass the differential clock signal to the plurality of load circuits 20a-20c. As is seen in FIG. 2 of Doblar, the fanout buffer 16 includes *several* buffer circuits 26a-26d that distribute the differential clock signal to the various memory modules 20a-20c. According to Doblar, each buffer circuit 26 includes emitter-coupled logic (ECL) circuits. By utilizing ECL circuits in each buffer circuit 26, noised immunity is improved when the ECL circuits are used in differential mode. (Col. 6, lines 1-28). As is shown in FIG. 2 of Doblar, each memory module 20a-20c is associated with a buffer circuit 26b-26d, and each buffer circuit 26a-26d is configured like the rest (FIG. 3). Accordingly, if a new memory module 20 is added, it too would be associated with its own buffer circuit 26.

Doblar fails to teach or suggest "buffering a differential clock signal with a single buffer circuit for a plurality of load circuits and configuring the single buffer circuit to adjust to alterations in the number of load circuits," as recited in claim 1. In the present invention, the single buffer circuit (FIG. 2, item 22) provides the differential clock signal to the plurality of load circuits. By using a single buffer circuit, as opposed to several in series, the number of load circuits can be increased without increasing signal noise.

In Doblar, FIG. 2 shows that the fanout buffer 16 includes a plurality of buffer circuits 26a-26d, as opposed to "a single buffer circuit." There is no teaching or suggestion that any of the buffer circuits 26 is configured to adjust to alterations in the number of load circuits because, as is shown in FIG. 2, each memory module 20a-20c is associated with a buffer circuit 26b-26d, and each buffer circuit 26a-26d is configured like the rest (FIG. 3). Accordingly, if a new memory module 20 is added, it too would be associated with its own buffer circuit 26, and none of the buffer circuits 26 would need to be adjusted.

In addition, Doblar fails to teach or suggest a configurable buffer circuit that "achieves a constant bandwidth and voltage level for the clock signal output while adjusting to alterations in the number of load circuits coupled to the configurable buffer circuit," as recited in claim 6. In Doblar, nothing teaches or suggests that the buffer circuits 26 are configured to make adjustments based on the number of load circuits coupled to it.

In the Office Action, the Examiner states that this feature is taught at column 4, line 28. That portion, however, discusses how the clock generator generates the differential clock signal and routes the complementary logic signals to the processor via separate signal lines. "The two signal lines conveying logic signals CK and CK' preferably have selected electrical impedances and uniform propagation delays (e.g., striplines or microstrip lines) such that signal reflections and skew are minimized." (Col. 4, lines 27-31). There is no mention of the buffer circuit.

Finally, Doblar fails to teach or suggest a buffer circuit comprising a differential amplifier circuit including a "programmable impedance circuit and a programmable current source circuit to provide a constant bandwidth and voltage level for a differential output clock signal," as recited in claim 13. In the Office Action, the Examiner states that Doblar's buffer circuit 26 has these features in FIG. 3. In particular, the Examiner indicates that Doblar's "differential amplifier input section" 28 teaches the present invention's programmable impedance circuit, and that Doblar's programmable current source is "(I)." According to Doblar, the differential amplifier input section 28 "may include a pair of bipolar transistors with collectors coupled to a positive power supply voltage and emitters connected together and coupled to a ground power supply potential. Differential amplifier input section 28 may receive the complementary logic signals CK and CK' of the differential clock signal." (Col. 5, lines 43-48). Nothing teaches or suggests that the "differential amplifier input section" is relevant to impedance, let alone a programmable impedance circuit. Moreover, the "I" in FIG. 3 merely shows current flowing to the ground power supply potential. Nothing teaches or suggests a programmable current source circuit, as recited in claim 13.

For the foregoing reasons, Applicants respectfully submit that claims 1, 6 and 13 are allowable over Doblar. Claims 2-5, 7-12 and 14-18 depend from claim 1, 6 and 13, respectively, and for that reason are also allowable.

Conclusion

In view of the foregoing, Applicants submit that claims 1-21 are allowable. Applicants respectfully request reconsideration and allowance of the claims as now presented.

Applicants' attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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